U.S. ATLAS Operations

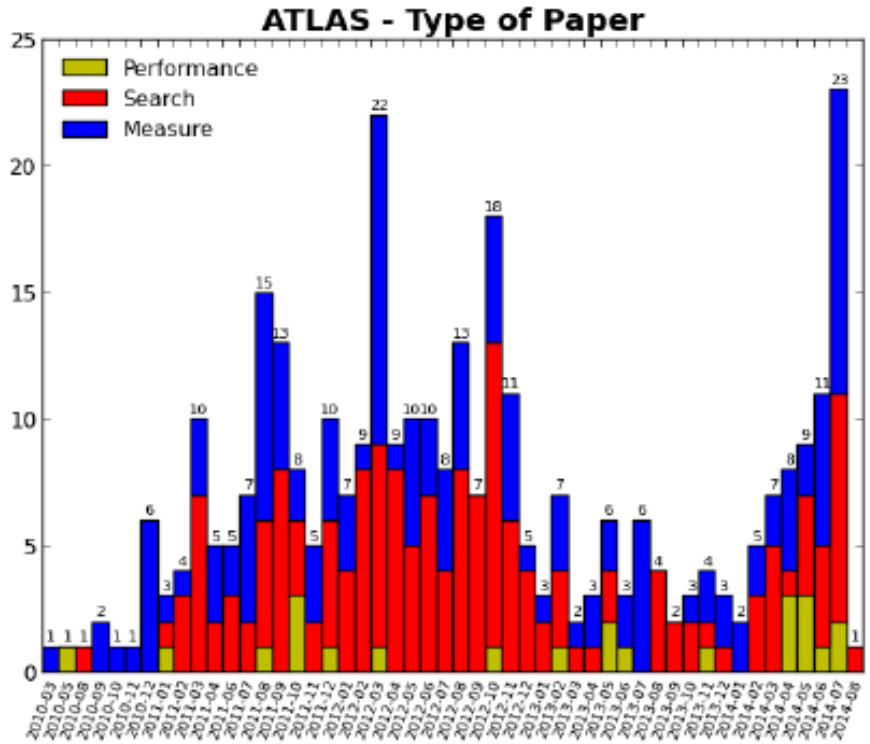
LHC Ops Meeting

August 12, 2014

News

- Director's Review of U.S. ATLAS Phase-II upgrade:
  - BNL, July 10-11, 2014
  - More details at the DOE/NSF Briefing on August 15, 2014.
- U.S. ATLAS Annual Meeting
  - Seattle, August 4-7, 2014

ATLAS Physics Publications:
339 papers to date
Highly productive month of July as
Run 1 data analysis is being wrapped up.

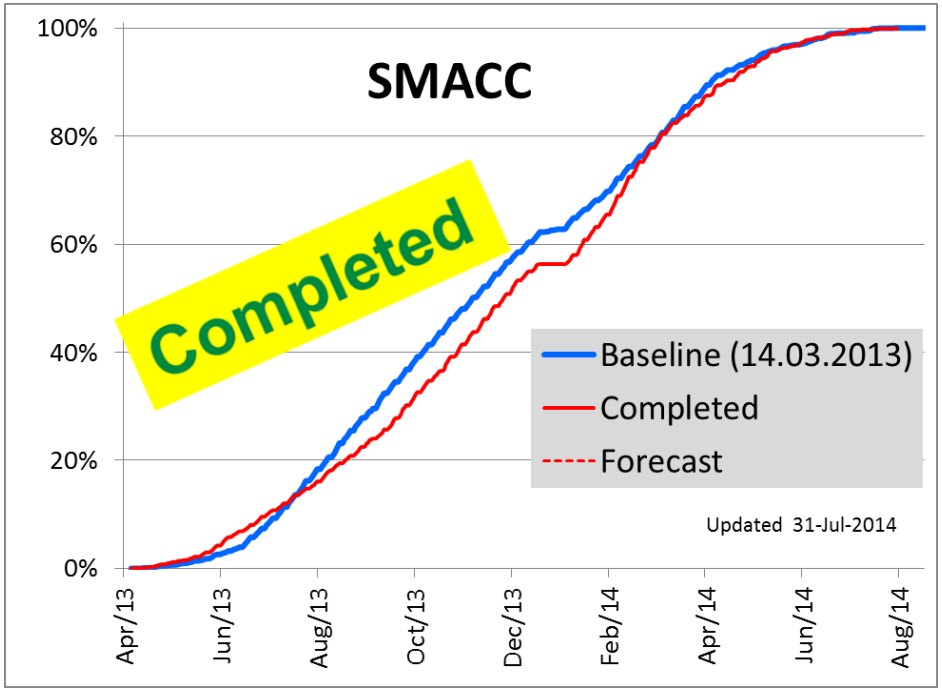


Maintenance & Operations

Hal Evans

Indiana University

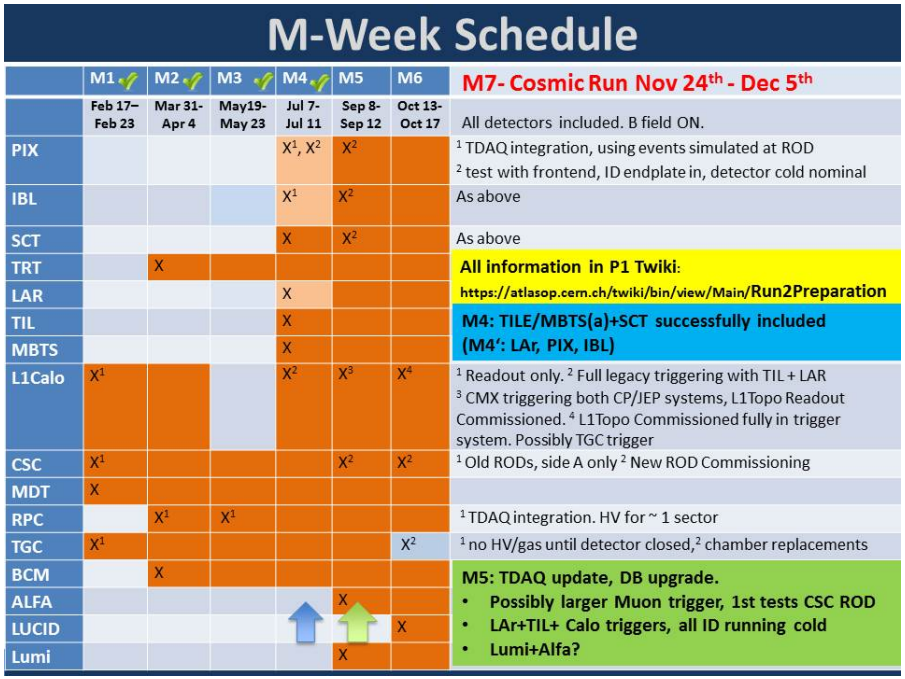
LHC Status



- Other progress
  - SPS: hardware tests proceeding as scheduled
  - LHC: sectors 6-7, 8-1, 1-2 in cooldown, last pressure tests finished 7/31, Copper Stabilizer Continuity Measurements (CSCM) complete in sector 6-7 (no problems found)
  - Still on track for LHC beam on in January 2015

ATLAS General

- Milestone Runs
  - M4 (July 7-11)
    - add: Calorimeters, Silicon (pixels, SCT, IBL), LAr
  - M5 (Sep. 8-12)
    - New CSC RODs, Calo Triggers, ID running cold



Silicon (A. Grillo)

- Unstable, intermittent operation of the Pixel heater control (part of the cooling system) discovered in early July:
  - Problem traced to flaky connectors that were installed when the control lines were cut in order to extract the Pixel package last year.
  - All the connectors were removed and replaced with splices over a few week period.
    - Effort led by UCSC technician F. Martinez-McKinney
  - Work completed just in time for ID End Plate re-installation
- SCT, Pixel and IBL cooling systems now all working properly.
  - A few leaks but at manageable levels
    - No worse than at during Run I.
- DCS operational – Interlocks re-enabled
- SCT, Pixels and IBL ready for ID End Plate reinstallation at end of July.
- Operating tests at normal operating temperature (i.e. cold) will start in mid-August after a few weeks drying out the ID volume.

TRT (M. Kruse)

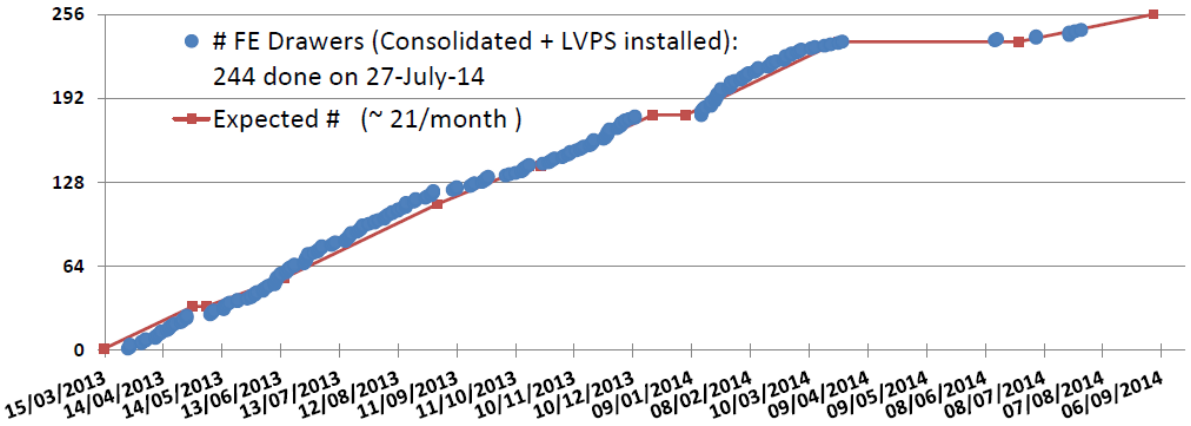
- TRT DAQ system running at >100kHz L1A rate demonstrated during M3, but still a lot of ongoing work:
  - read-out with high-occupancy
  - various calibrations and optimizations (e.g. threshold levels)
  - integrated tracking with Silicon systems
    - full tracks should be available for first time from cosmics end of September
- Ar/Xe Gas mixture optimization
  - Studies optimizing cost versus PID ongoing
  - Effect on electron identification efficiency now better understood
  - Plan to finish by Sept/Oct
    - so TRT simulation and digitization can be frozen by Oct/Nov 2014

LAr (J. Parsons)

- Subsystem is stable, with regular calibrations being done in advance of starting soon to close the detector

- After Phase 1 Demonstrator successfully installed in one barrel crate (I06), continued commissioning is underway
  - Performance of readout path (noise, etc.) is same as neighboring crates, so there seems to be no adverse impact
  - Installation of Demonstrator backend electronics in USA15 is proceeding, so soon can start to read out new trigger path

TileCal (J. Proudfoot)



244 drawers consolidated until 27th July 2014

Commenced consolidation of last remaining modules

- Re-opened modules identified as having a high priority problem: LBC25, LBA07, LBA17, EBC42, EBC58.
  - Next candidates: EBC39, LBC58
  - There are no more modules in URGENT priority list for re-opening.
- Migration of Tile Conditions Online DB to the new instance CONDBR2 (with some schema tuning/ modification) proceeding well.

Muons (B. Zhou)

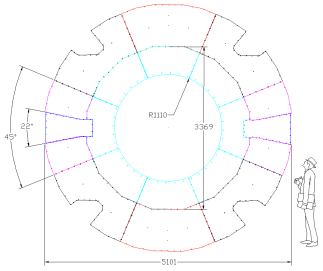
- MDT (WBS 3.5.1)
  - Small Wheel C re-commissioning successfully finished – reaching an important milestone
    - Replaced a Mezzanine (EIL1C05) and a CSM (EIL1C03)
    - No gas leaks (<5mbar/day) ; All chambers hold HV 3080V with low dark current
    - Check/tested all connectivity mapping for LV, HV, DAQ and DSC Monitor
    - Measured tube noise level and found all are below specification and no unexpected dead tubes
    - Integrated into MDT TDAQ, ready for M5
  - Other maintenance accomplishments
    - Fixed a damaged cover on MDT chamber; HV trips on 4 chambers; a fiber problem on EO chamber
    - Test all MDT readout mapping, fixed a pair fiber mis-connection on MRODs for barrel chambers
- CSC (WBS 3.5.2)
  - Install new fibers to replace damaged one on Wheel A; Retested readout of both wheels:
    - Wheel A: Sector 5 has one ASM (192 channels) not working: because of a broken fiber which was replaced but need a special patch cord to remap channels on RODS which will restore 100% operation.
    - Wheel C: 100% operational
  - New CSC ROD boards for one endcap are ready and installed at CERN
    - 2nd half is produced and will be sent to CERN soon.
    - TDAQ interface and SCA controller demonstrated; TTC clock recovery successful; on schedule for M5
- Endcap alignment (WBS 3.5.3)
  - New alignment devices on all BEE sectors are fully commissioned --reaching an important milestone!
    - The remaining work is to adjust the BCAMs mounted on the Small Wheel (EIS sectors) so that they “see” the sensor that are mounted on the BEE chambers, waiting all detector/ECT in final places
  - All other parts of the systems have been fully tested and are operational.

    14 pre-prod COBs in ROD ATCA shelf

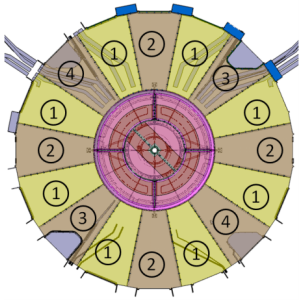
TC (V. Polychronakos)

- New Inner Detector Endplate: BNL & CERN design
  - Decision not to install nIDEP was made in May
    - difficulties with services feed-throughs (CERN part of design)
  - Instead, plan was to test three plates in ATLAS during re-installation of old design
  - Test of new plates was just done during last weeks
    - have not received official CERN report but have been told that test was successful.

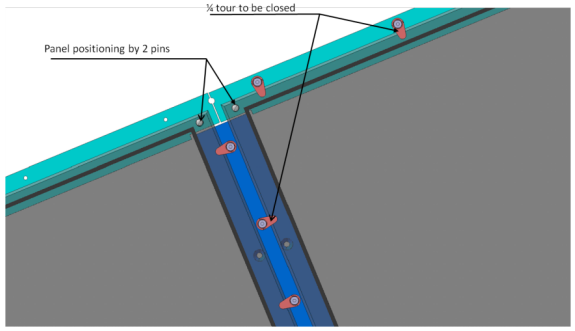
Old design



New design

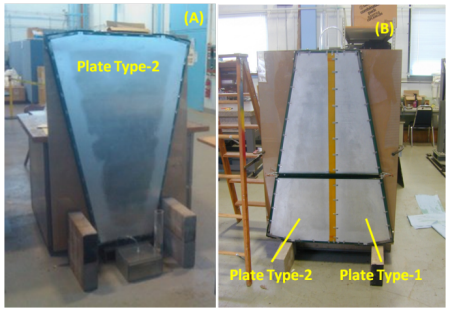


New design uses fasteners for quick installation/removal



Installation test at BNL

Leak testing



Software & Computing

Torre Wenaus (BNL)
Mark Neubauer (UIUC)

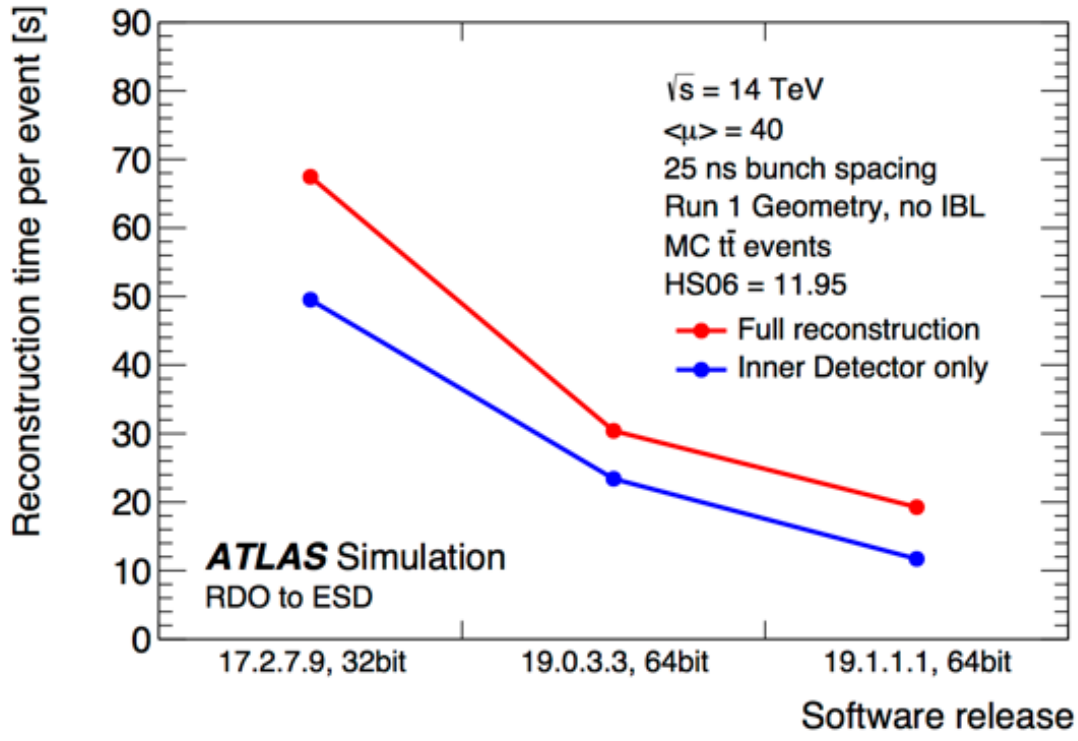
Software & Computing Update

- Smooth production operations grid-wide, ~full utilization at ~150k concurrent jobs (peaks now close to 180k), heavy simulation production
- Data Challenge 14 (DC14) in full swing, close to schedule, next major phase is bulk xAOD production
- US Facilities readiness for DC14 and Run 2 is good, performing very well
- New ATLAS data management strategy nearing completion
- ATLAS computing report to WLCG Computing Scrutiny Group nearing completion
  - Will describe the new strategy
- **3x speedup – the target on which our resource requests are based – achieved for reconstruction software**
- HPCs beginning to deliver at a significant level: ~5k slot equivalent ATLAS-wide in recent months
- Good progress on US deliverables from LS1 development
  - Transition to new PanDA extension JEDI for distributed analysis takes place this week
  - Prodsys2 coming online for a growing slate of workflows, most recently reprocessing
  - Bulk production of xAODs will begin soon, users eager to pick them up for xAOD based analysis

S&C Update (2)

- Very successful US ATLAS Physics Workshop last week in Seattle
  - Comprehensive set of reports in plenary and parallel from S&C, physics support people
  - Tier 3 implementation committee presented preliminary results, lively discussion ensued
    - Discussion continues this week in operations program management
    - Will be presented to JOG in September
- Interesting US ATLAS Software & Computing/Physics Support meeting coming Aug 20-22 at LBNL
  - Facilities, software planning, physics support, scrubbing in one efficient meeting
  - Technical face-to-face focused on four topics: meeting needs of US analysis (eg. Tier 3 support), ROOT based analysis ecosystem, HPCs, event service, plus a facilities session; all plenary, almost 50 people

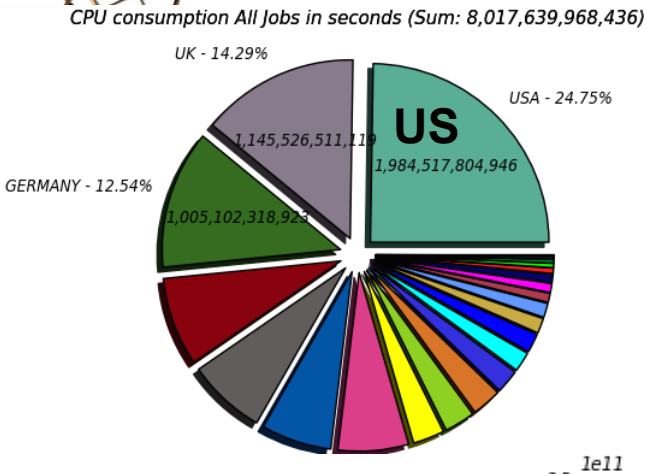
3x Reco Speedup Achieved

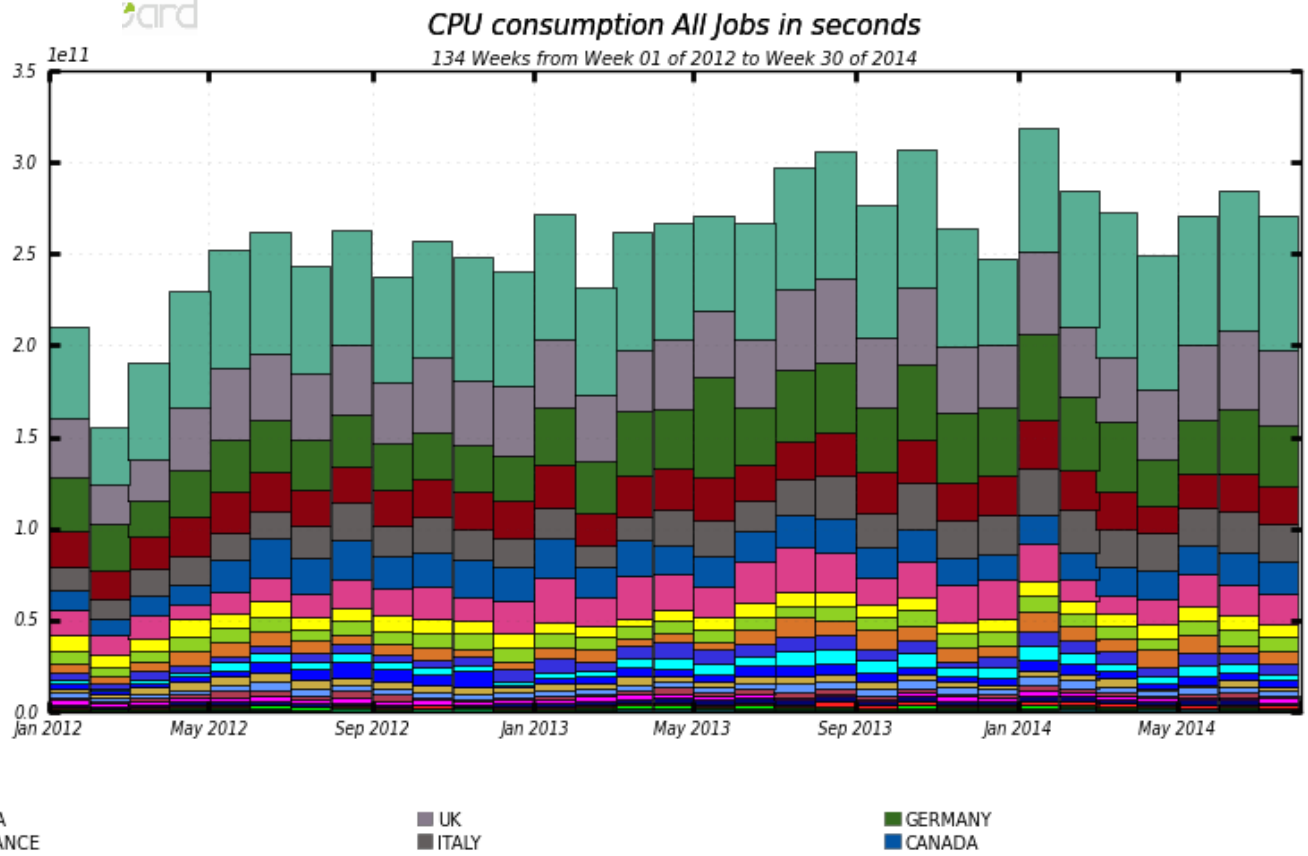


Run 1 release

Run 2 release

Sustained Usage Since 1/2012





C-RSG Report - CPU

Figure 1 shows the CPU usage and number of pending jobs for the period 1st April to 31st July 2014. The usage peaks at close to 200,000 slots. The sum of pledges corresponds to approximately 100,000 slots

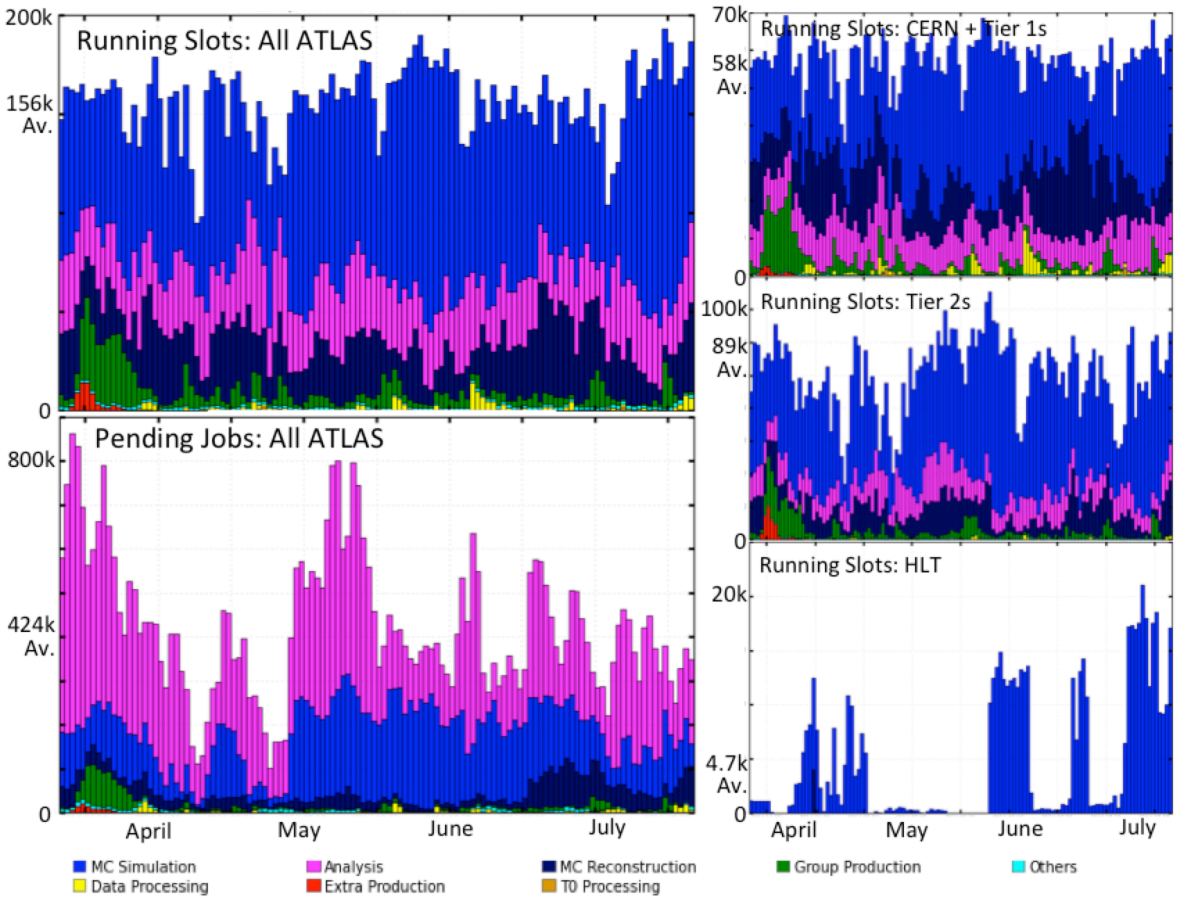


Figure 1: Slots of running jobs and number of pending jobs for the period 1st April to 31st July 2014

C-RSG Report - Disk

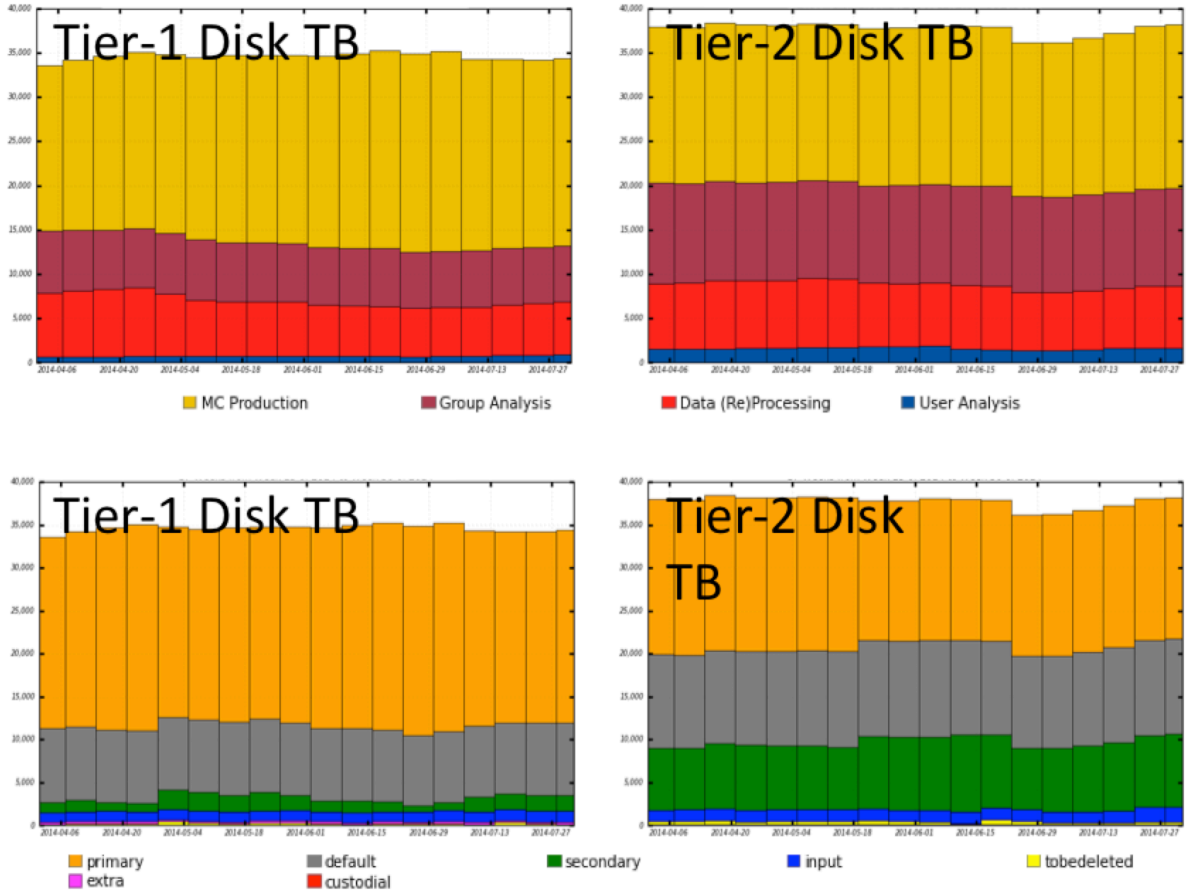
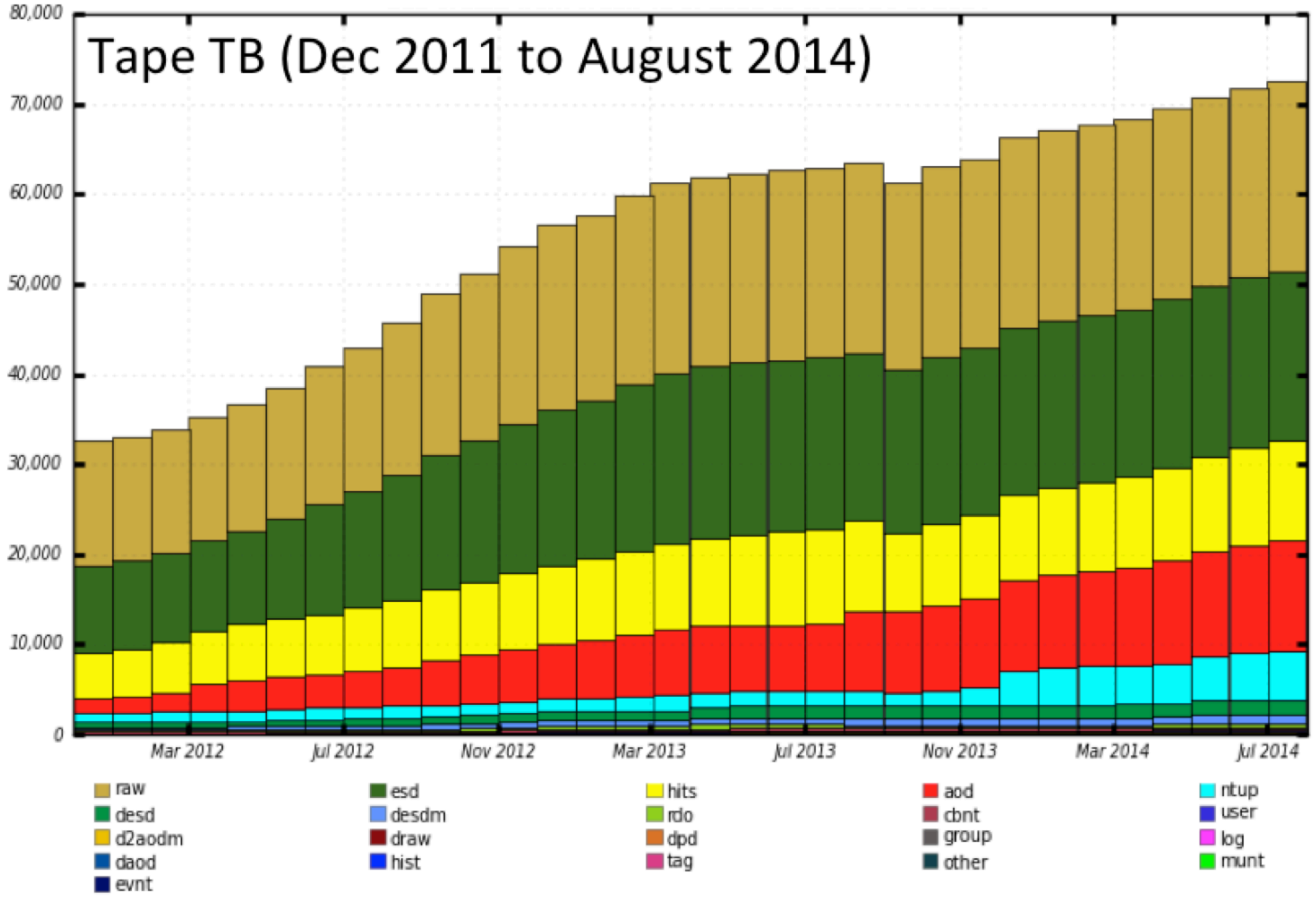


Figure 2: Disk usage at Tier 1s and Tier 2s for the principal types of ATLAS data for the period 1st April to 31st July 2014. The upper plots show the breakdown by types of data; the lower plots show the breakdown by replica class

C-RSG Report - Tape



Physics Support Update
J. Nielsen, E. Varnes

- Pilot xAOD datasets (Run 1 MC) are available for testing and tutorials
  - These will be brought to the U.S. facilities' LOCALGROUPDISK for easy access
  - Working in physics groups to reduce size of skimmed xAOD group datasets (most are already <5% of total xAOD size, but some outliers need work)
- Many U.S. ATLAS physicists have attended "xAOD mini-tutorials" recently, including remote events at the Analysis Support Centers
  - LBNL (July 22-25); very positive feedback
  - BNL (Aug. 27-29)
  - ANL (Oct. 28-29)
  - Formalized setup of remote software tutorials, including video-on-demand lectures
- Physics Support working together with U.S. ATLAS Facilities Integration to develop testing suite of real-life analysis software examples
  - Will be used to monitor performance of FAX wide-area data access and new ATLAS Connect cluster service that extends local HTCondor queues to facilities
  - Test code will be accessible by cloud VM instances and remote Tier 3 systems
  - Expecting this to become part of new ATLAS distributed analysis analytics platform

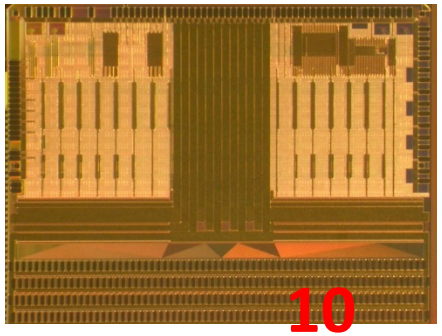
Upgrade R&D

Alex Grillo for Abe Seiden
UC Santa Cruz

Upgrade R&D Update
On Chip-Set for Strip Tracker

Status Report: Chip set (front-end and controller chip) for new strip tracker. These are among the major items under development by the R&D program, required for ATLAS to be ready for tracker construction. Initial error in front-end found and we report on subsequent work.

ABC130
256 Channel Strip Front End Chip



Focused Ion Beam repair successful

FIB'd ABC130 chips bonded to Hybrid & Sensor.

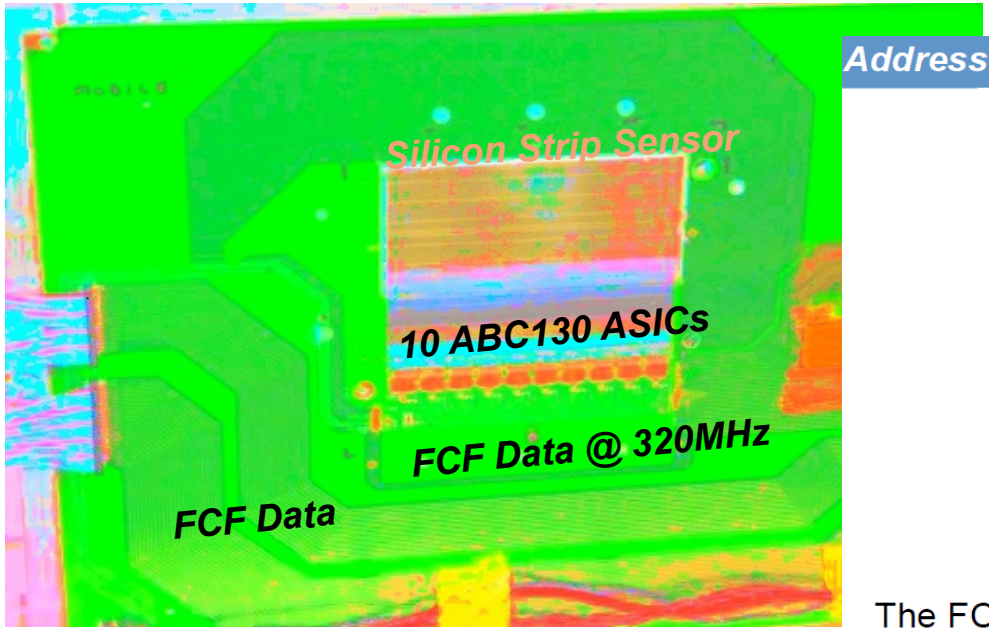
- All chips configure properly. Chip termination OK
- Serial chain readout OK @80MHz
- Typical power 85mA/chip. Analog voltages OK: (Regulator, Band Gap)
- Gain variation acceptable but larger than expected from simulations.

5 revised ABC130 wafers returned from IBM.

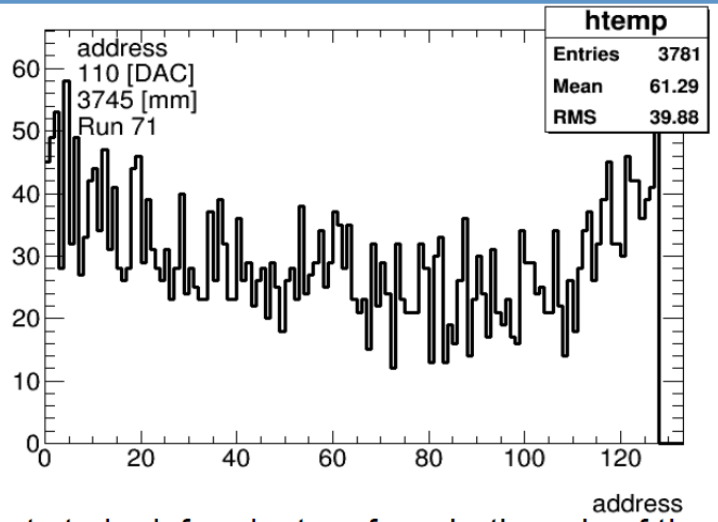
- **90% yield 1st wafer.** → 5 wafers estimated that we will get 610 yielded parts.
- Gain variation larger than expected, consistent with **FIB'd** parts.
- No known problems so far.
- Waiting on results from first bonding of new ABC's to a PCB.

ABC130 Tests at LBNL Using SLAC Test Beam Data

Successfully used sensor plus ABC130 at SLAC in test beam to demonstrate Self Seeded Trigger and explore chip gain question. First results show FCF (cluster finder on chip) behaves as expected for establishing the self-seeded trigger.



Address of the correlation



The FCF starts to look for clusters from both ends of the 128 strips, whenever there are two clusters, it stops. This is optimized for the HL-LHC occupancy. The ESTB is much more intense, which leads to a "bias" of correlation address.

We are making good use of the SLAC test beam. Also earlier tests by Japanese groups.

Production Plans for ABC130's

- Prototyping plans for staves require 6000 to 7000 ABC die. Assuming 120 yielded die/wafer → ~ 58 wafers have to be produced.
- 2 Production runs in planning, first as soon as presently planned tests are complete.
- No quotes yet, but we assume between 2 and 3K/ wafer.

Hybrid Controller Chip (HCC) Status

- Postponed May 18 Submission date.
  - Corrected an addressing issue picked up in 4/24/14 review.
  - Revised resets to match collaborator requests.
  - Continued to improve Place & Route scripts.
  - Significant reduction in the number of unresolved compilation errors/ warnings. 1000's → 10's.
  - Test coverage increased from basic functionality .
  - Improved specification.
- Follow up Review @ CERN 16 July 2014 (ATU-TC-ER-0024)
  https://indico.cern.ch/event/327089/
- Green light for submission some recommendations made:

→ Most important work ahead, more simulation

HCC Status

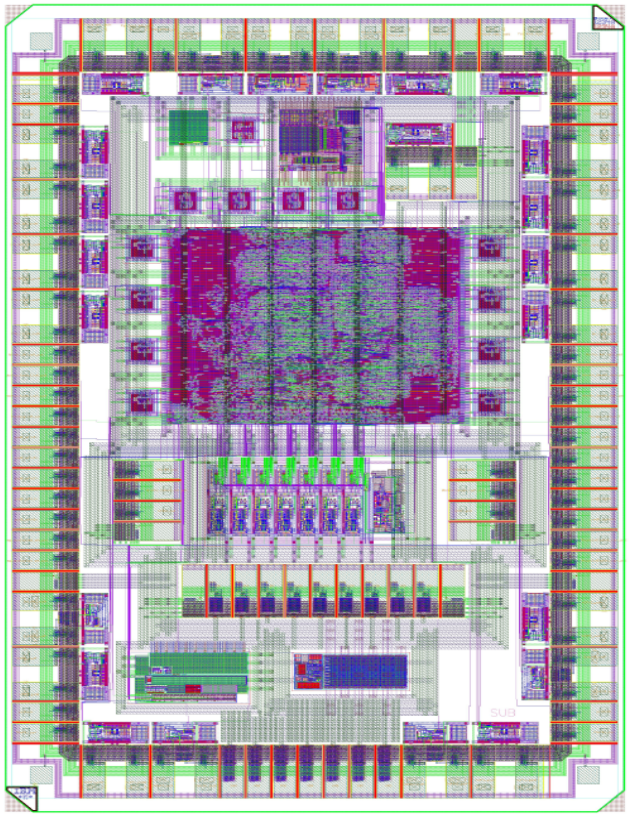
Submission Date: August 18 to MOSIS

Collaborative Effort led by Penn:
US Institutions: Penn, UCSC
Europe: CERN, RAL, Geneva, Krakow

Chip Contains:

- Command Decoder, Resets, ABC130 Command & Control
- Data Concentrator with 160 or 320Mbps Outputs
- 8b/10b output option
- 99 pads in a Dual pad-ring to fit onto Hybrid
- Standard Cells: ~40,000 Nets: ~45,000
- Macros: (Analog & Digital Blocks)
  - **Band Gap, Voltage Regulator**
  - **PLL /w 40, 80, 160, 320, and 640MHz**
  - Delay Macro Coarse & Fine (6, 0.6 ns)
  - Autonomous Monitor (Voltages & Temp & HV)
  - Power-on Reset, Radiation intensity Interlock
- **Script driven Silicon Compiler for Place & Route**
- (based on CERN code) ~ 3600 lines of code
- **Cadence Verification: Verilog, Encounter, Spectre**
- **Calibre Error checking @ UCSC**
- **Timing margin (post layout parasitics) under study.**
- **UCSC & RAL test bench will be used to test/qualify HCC with multiple ABC130's**

Dimensions: 4700X2860um



HCC MPW Costs

- Submission through Foundry services at CERN
- Files will be sent directly to MOSIS.
- 40 die → 40.7K CHF.
- 40 additional die ~1/3 of MPW cost.
- COST for first 80 die $50 - 54K CHF.

→Covers use of first 800 ABC130s'. Only about 610 ABC130 die available from 5 revised wavers.

Plan for the ~600 HCC required to service 6-7K ABC's will be made after testing of first HCC's.